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S/N 09/460,742 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Rajendran Nair et al.	Examiner: Jung Kim	
Serial No.:	09/460,742	Group Art Unit: 2816	
Filed:	December 14, 1999	Docket: 884.229US1	
Title:	DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION		

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on July 12, 2001. Please amend the above-identified patent application as follows.

This response is accompanied by a petition, as well as the appropriate fee, to obtain a three-month extension of the time period for responding to the Office Action, thereby moving the deadline for response from October 12, 2001 to January 12, 2001.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 4, 9, 10, 14, and 16. The specific amendments to individual claims are detailed in the following marked up set of claims.

4. [Amended] A circuit comprising:

a voltage node;

a ground node; and

a transistor including a gate, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node [coupled between the voltage node and the ground node], the [transistor including an] gate comprising a p-type polysilicon [gate is] , wherein the transistor is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value. [\]

9. [Amended] A circuit comprising: